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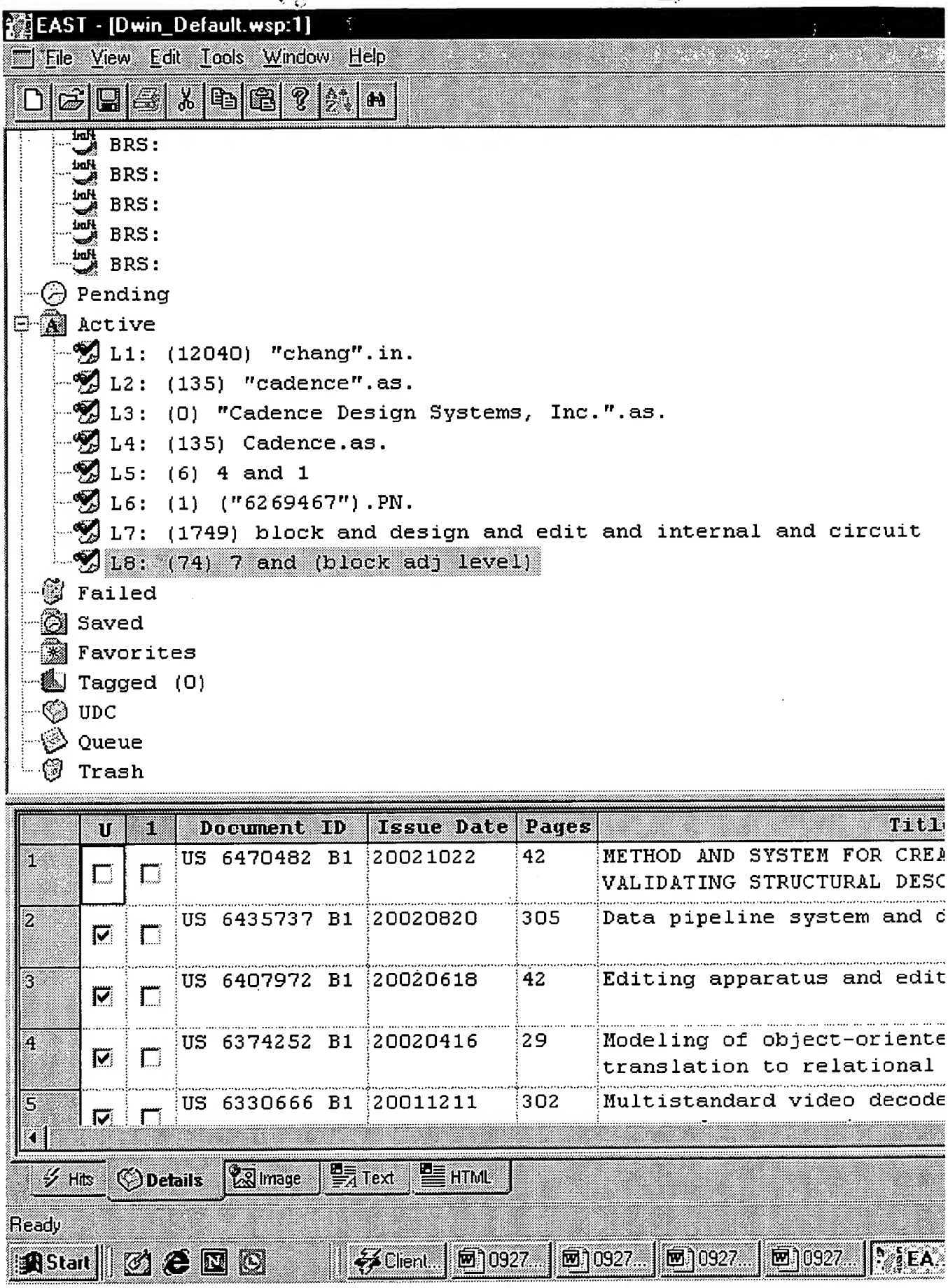
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L3: (0) "Cadence Design Systems, Inc.".as.
L4: (135) Cadence.as.
L5: (6) 4 and 1
L6: (1) ("6269467").PN.
L7: (1749) block and design and edit and internal and circuit
L8: (74) 7 and (block adj level)
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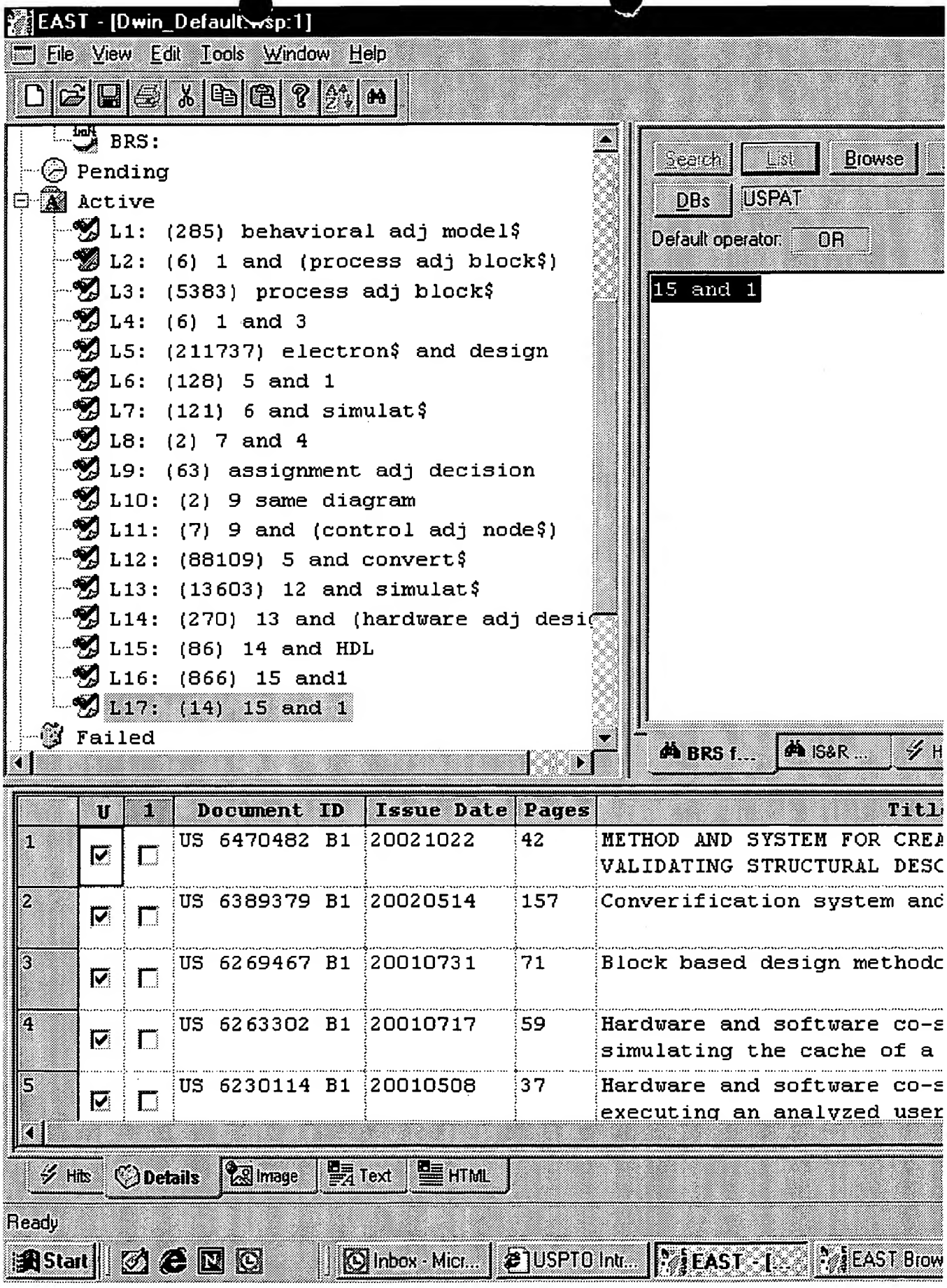
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L7: (121) 6 and simulat$
L8: (2) 7 and 4
L9: (63) assignment adj decision
L10: (2) 9 same diagram
L11: (7) 9 and (control adj node$)
L12: (88109) 5 and convert$
L13: (13603) 12 and simulat$
L14: (270) 13 and (hardware adj desi
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1 US 6470482 B1 20021022 42 METHOD AND SYSTEM FOR CREA VALIDATING STRUCTURAL DESC
2 US 6389379 B1 20020514 157 Converification system and
3 US 6269467 B1 20010731 71 Block based design methodc
4 US 6263302 B1 20010717 59 Hardware and software co-s simulating the cache of a
5 US 6230114 B1 20010508 37 Hardware and software co-s executing an analyzed user
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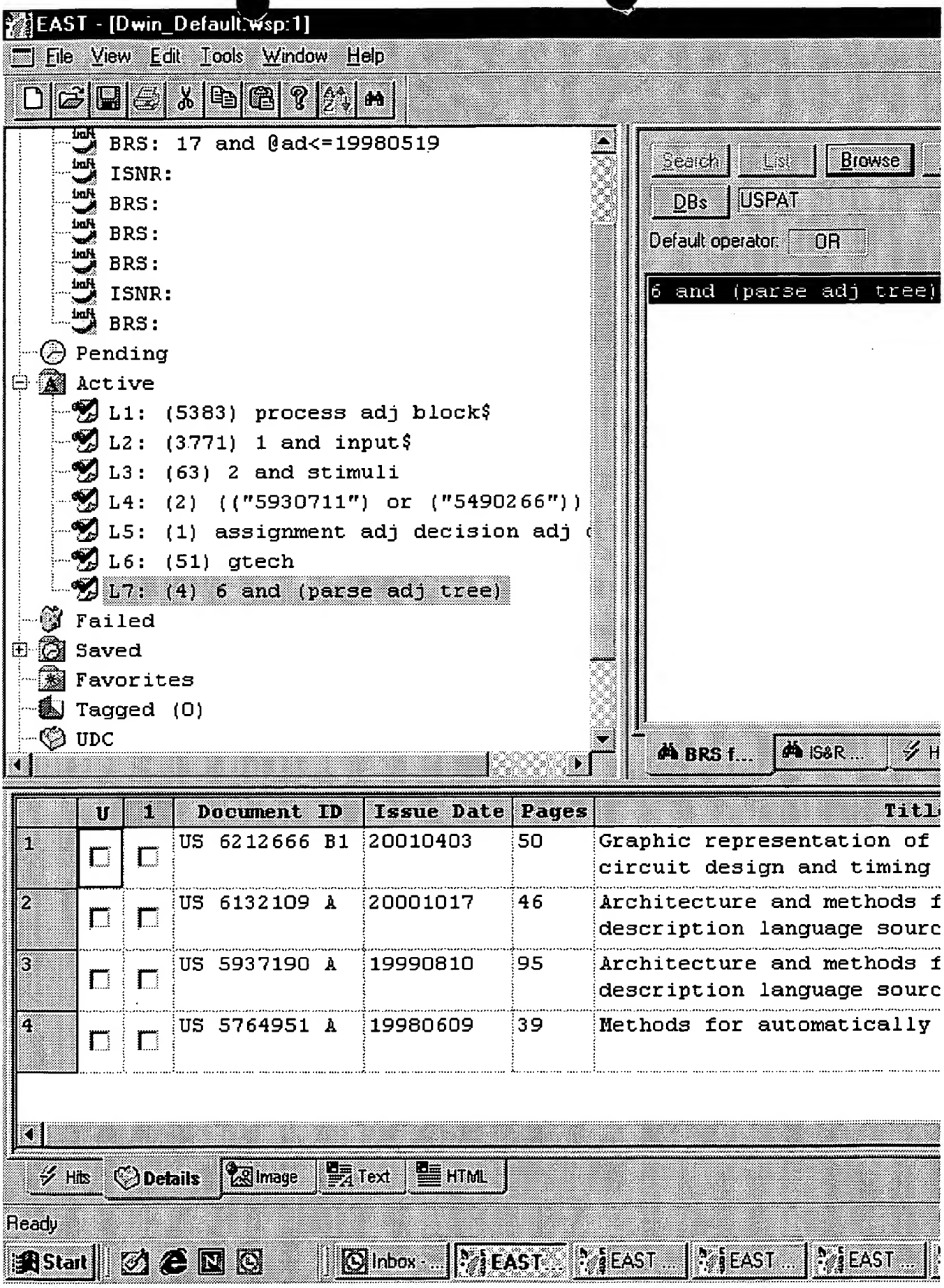
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1 US 6212666 B1 20010403 50 Graphic representation of circuit design and timing
2 US 6132109 A 20001017 46 Architecture and methods f description language sourc
3 US 5937190 A 19990810 95 Architecture and methods f description language sourc
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